

RECEIVED  
CENTRAL FAX CENTER

OCT 24 2006

IN THE CLAIMS

1. (Original) A method comprising:  
computing an energy delay<sup>2</sup> product metric for a current architecture configuration over a predetermined period of time;  
comparing the computed energy delay<sup>2</sup> product metric to an energy delay<sup>2</sup> product metric of a prior architecture configuration to determine an energy effectiveness of the current architecture configuration; and  
adjusting a number of active instruction schedulers of the current architecture configuration according to the energy effectiveness of the current architecture configuration.

2. (Original) The method of claim 1, wherein computing the energy delay<sup>2</sup> product metric comprises:

selecting an active instruction scheduler from one or more active instruction schedulers of the current architecture configuration matching a selected instruction scheduler type;

computing an energy consumption value for the selected instruction scheduler and one or more associated logic elements as a product of an access count and a predetermined energy per access amount of the selected instruction scheduler and the predetermined period of the time squared;

repeating selecting of the instruction scheduler, computing of the energy consumption value and storing of the energy consumption value for each instruction scheduler of the current architecture configuration matching the selected instruction scheduler type to form an energy consumption sum;

storing the energy consumption product sum for the instruction selected scheduler type;  
and

repeating the selecting the active instruction scheduler, computing of the energy consumption product, repeating, and storing the energy consumption product for each instruction scheduler type of the current architecture configuration to form the energy consumption value of the current architecture configuration.